CASPaR

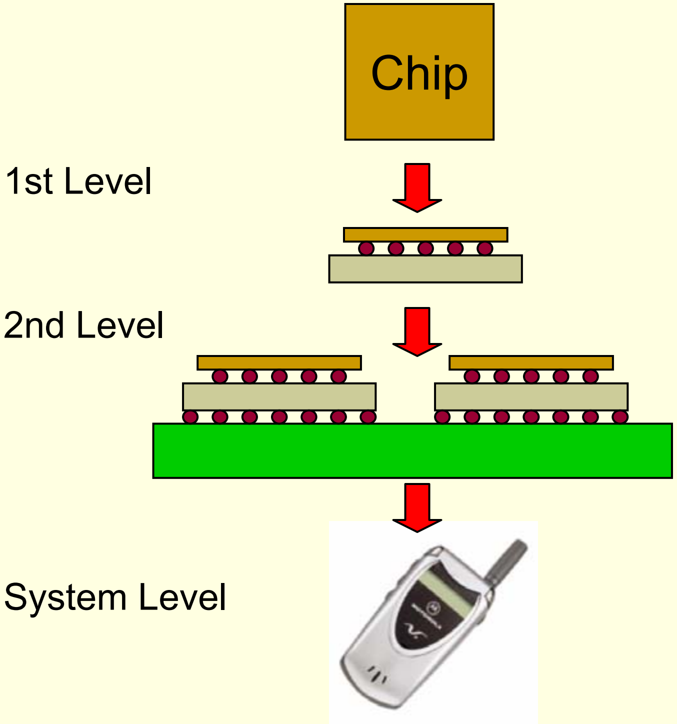
Off-Chip Interconnects: Design, Fabrication, and Reliability

Suresh Sitaraman, Ph.D.
Professor, The George W. Woodruff School of Mech. Eng.
Director, Computer-Aided Simulation of Packaging Reliability Lab
Georgia Institute of Technology
Atlanta, GA 30332-0405
Phone: 404-894-3405; FAX: 404-894-9342
email:suresh.sitaraman@me.gatech.edu

Georgia Tech

Packaging Needs

- ITRS predicts 15 μm pitch requirement (peripheral) by 2016
- Need for ultra fine pitch chip-to-next level interconnects



Year of Production	*2003*	*2005*	*2007*	*2010*	*2013*	*2016*
MPU Physical Gate Length (nm)	45	32	25	18	13	9
Chip Size (mm2)						
High Performance	310	310	310	310	310	310
Package Pincount						
High Performance	2057	2489	3012	4009	5335	7100
Chip Interconnect Pitch (µm)						
Wire bond –ball	35	25	20	20	20	20
Flip chip (area array for cost performance and high performance)	***150***	***100***	***80***	***70***	***70***	***50***
Peripheral flip chip for hand-held, low cost, and harsh	***60***	***40***	***30***	***20***	***20***	***15***

"ITRS Technology Roadmap for Semiconductors -- Assembly and Packaging", public.itrs.net

Georgia Tech

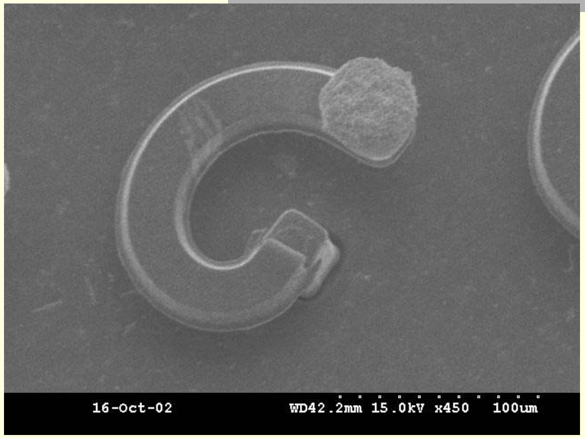
Off-Chip Interconnects: Requirements

- 20 mm x 20 mm die
- Large number of I/O – 8000 and above
- Silicon on organic substrates – 40 micron lateral displacement over 200 C
- Vertical displacement 10 micron to accommodate substrate non-planarity
- At least 7 mm/N compliance for low-K/Cu dies so as not to delaminate or crack low-K dielectric
- No underfill attach and reworkable
- Fatigue life 1000 cycles (-55 to 125 C)
- Environmentally friendly
- Low electrical parasitics
- Wafer-scale and cost-effective
- Scalable pitch
- Standard IC fabrication process and infrastructure
- Reproducibility and uniformity
- High-yield

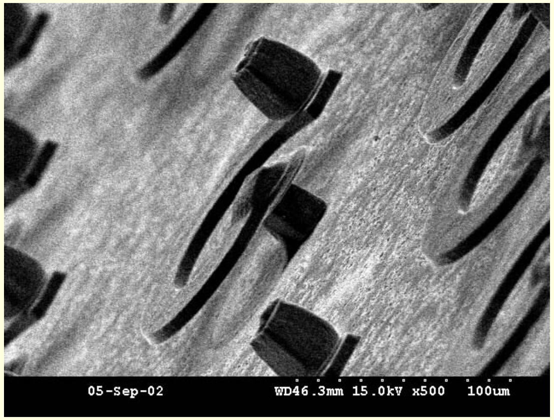
A Potential Solution:
Helix-type Compliant Off-Chip Interconnect

- This novel technology is being developed by Georgia Tech
  - U.S. patent pending

- Characteristics
  - Helix-like *completely free-standing* copper structure
  - *Compliant*
  - LIGA-like *wafer-level batch process*
  - Photolithography enables *fine pitch*
  - Free-air package with *no underfill and no elastomer*
  - *Improved thermo-mechanical reliability* compared to solder bump interconnect with no underfill

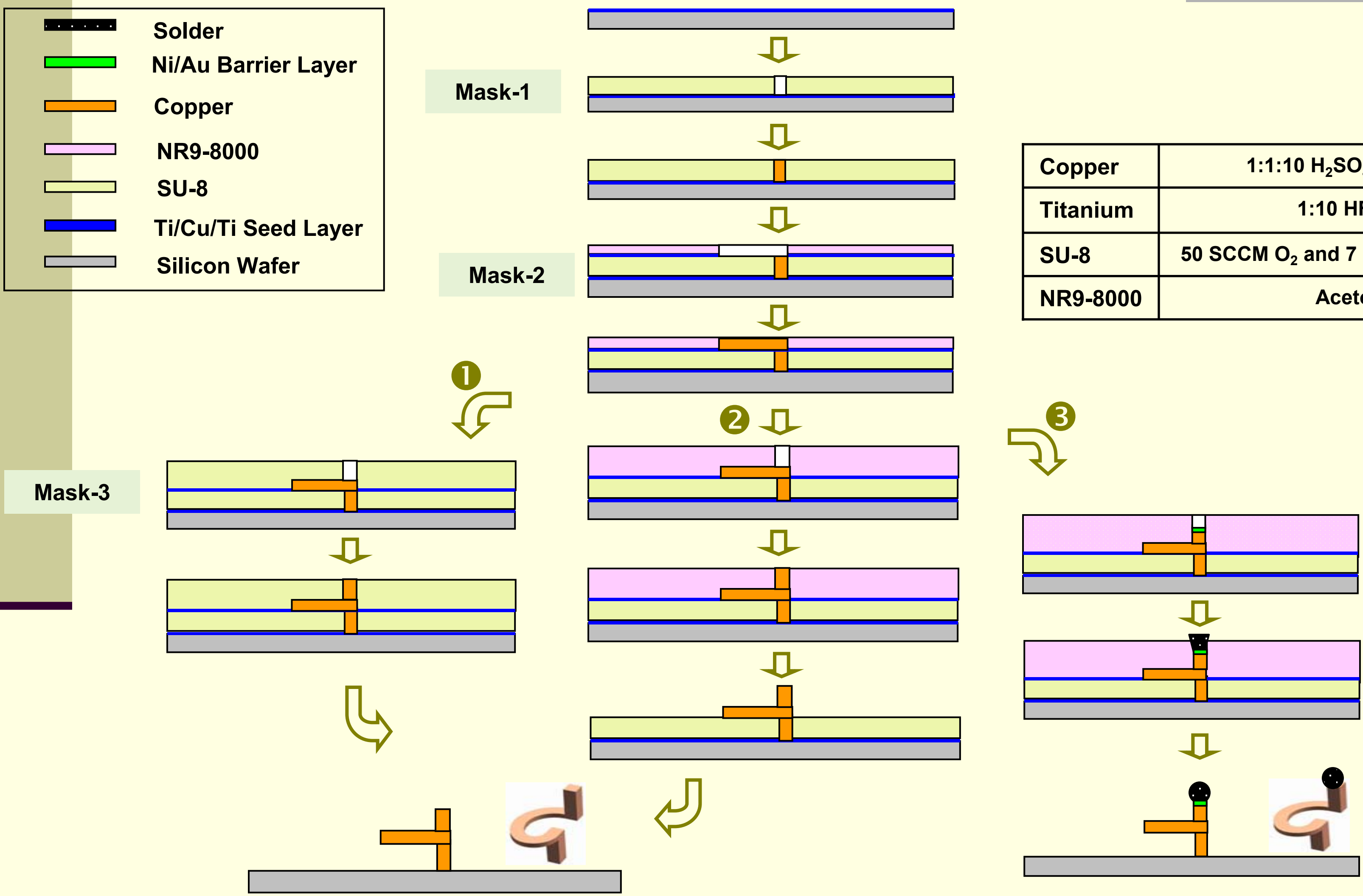


G-Helix Interconnect



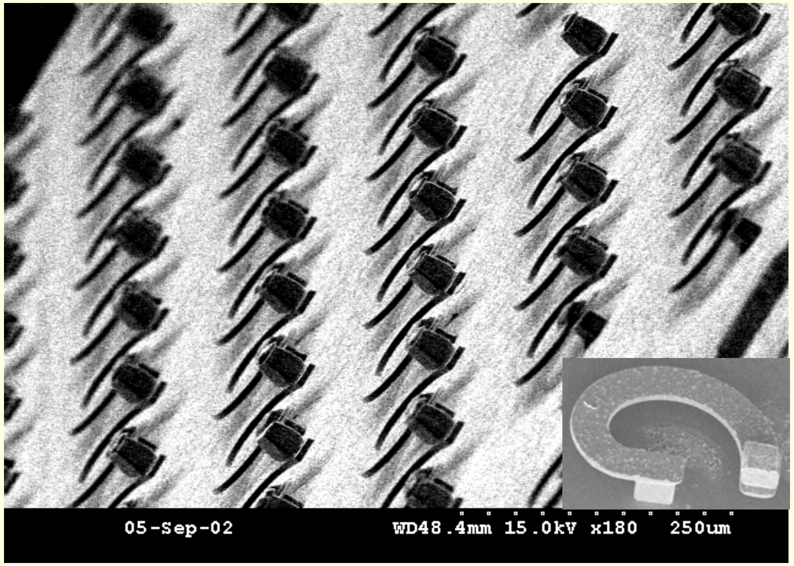
G-Helix Interconnect

G-Helix Interconnect Fabrication – Process Flow

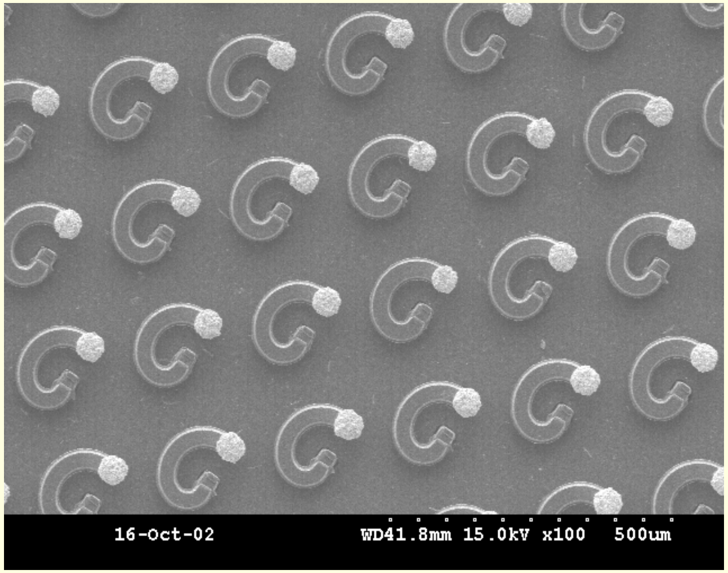


Copper	1:1:10 $H_2SO_4/H_2O_2/H_2O$
Titanium	1:10 HF/H_2O
SU-8	50 SCCM O_2 and 7 SCCM CHF_3 (RIE)
NR9-8000	Acetone

G-Helix Interconnect Fabrication – Results



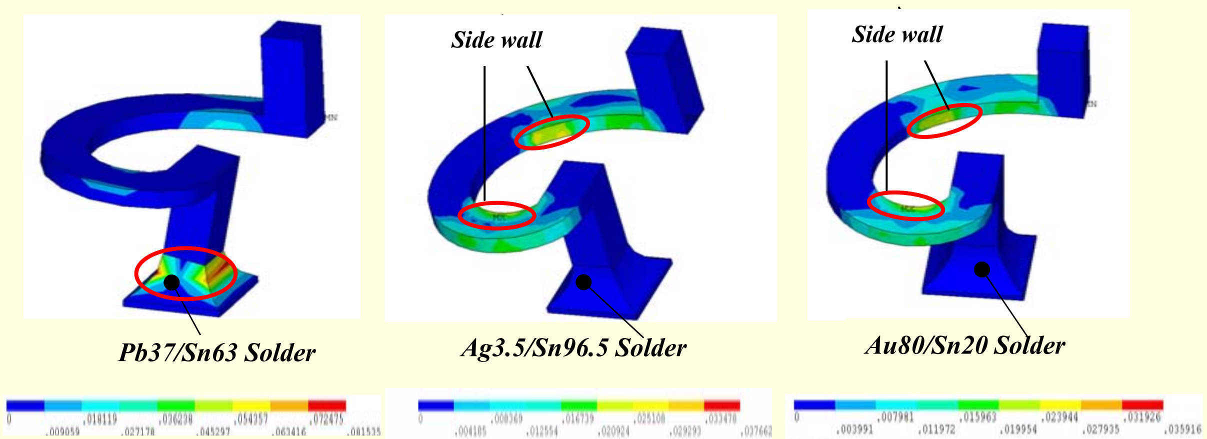
Area-array 3-layer G-helix Interconnects with 200μm pitch



Area-array G-helix Interconnects with Pb/Sn Solder

- Zhu, Q., Ma, L., and Sitaraman, S. K., "Design and Fabrication of β-fly: a Chip-to-Substrate Interconnect," IEEE Transactions on Components and Packaging Technologies, Vol. 26, No. 3, September 2003, pp. 582-590.
- Zhu, Q., Ma, L., and Sitaraman, S. K., "Design Optimization of One-Turn Helix - a Novel Compliant Off-Chip Interconnect," IEEE Transactions on Advanced Packaging, Vol. 26, No. 2, May 2003, pp. 106-112.

Effects of Solder Paste Material: G-Helix Interconnect Package



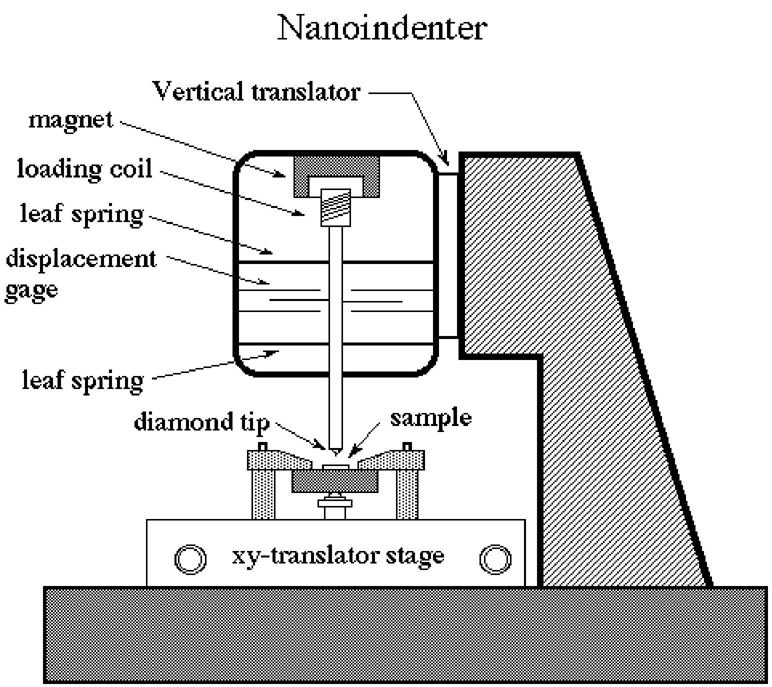
Accumulative Plastic Strain in the Outermost G-Helix Interconnect and Solder Paste

G-Helix with Pb37/Sn63	Max. $\Delta\varepsilon_{plastic}$ (%)	4.6521 (in solder)
	Predicted Fatigue Life	85
G-Helix with Ag3.5/Sn96.5	Max. $\Delta\varepsilon_{plastic}$ (%)	0.5061 (in copper)
	Predicted Fatigue Life	1038
G-Helix with Au80/Sn20	Max. $\Delta\varepsilon_{plastic}$ (%)	0.4724 (in copper)
	Predicted Fatigue Life	1165

Experimental Method

- Titanium thin film is deposited on a 6-inch Silicon wafer by DC Sputterer technique at 6 millitorr Argon pressure.
- The base pressure is about 6.5 x10^{-6} Torr.
- The Ti target size is 3 inches.
- The deposition rate is 1 Å /s ± 6.2%.
- Thickness of the Ti thin film on Silicon substrate is about 600 nm measured using an ellipsometer.
- The internal stress is 100 MPa compressive

Nanoindentation Tool Setup

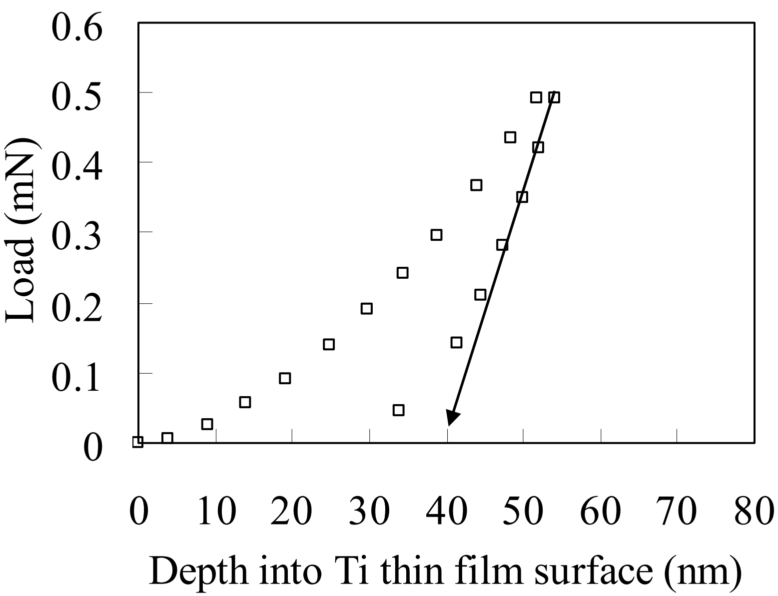


- Indenter: Berkovich shaped diamond indenter
- Load resolution: 0.1 mN
- Displacement resolution: 0.2 nm

Load-Depth Experimental Data

- All the data points were averaged from data at six independent locations to determine the mechanical properties of the Ti thin film.
- The loading part is elastic-plastic, which is used to characterize the plastic properties
- The unloading part is elastic dominant, which is used to obtain Young's modulus by:

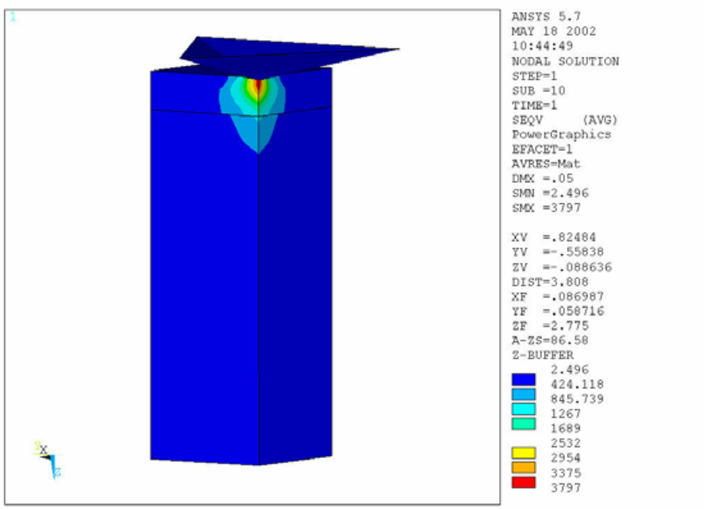
$$E_{TF} = \frac{\left(1 - \upsilon_{TF}^{2}\right) E_r E_i}{E_i - (1 - \upsilon_i^{2}) E_r}$$



The depth is 50nm of the 600nm thickness

Finite Element Modeling

- The contact element is applied on the surface of the nanoindenter tip and the indented surface of the Ti thin film.
- Since the young's modulus of the indentor (≈1140 GPa) is about an order of magnitude higher than that of the Ti thin film, the nanoindentater is assumed to be rigid in the finite element modeling.
- Multilinear isotropic hardening plasticity model is used in the finite element simulation.



Characterization of Mechanical Properties of Thin Films

- The internal stress in the Ti thin film about compressive 100 MPa is incorporate in the finite element modeling of nanoindentation process

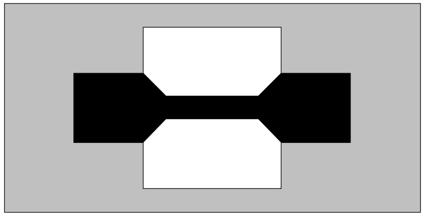
Material	Test method	Young's modulus	Yield Stress	Strain hardening exponent
Titanium	Thin film (Nanoindentation & FEM)	128 GPa	700 MPa	0.35
Titanium	Bulk (Handbook)	120 GPa	200 – 400 MPa	0.14

Shan, Z. and Sitaraman, S. K., "Elastic-Plastic Characterization of Thin Films using Nanoindentation Technique," Thin Solid Films, 2003, Vol.437, pp. 176-181.

NanoUTM®

The properties of thin films have not been investigated as much as those of bulk mainly because of:

- limitation of available equipment for the measurement of small loads and deflections.
- complexity of sample design and preparation.



Recently Developed
MTS- Nano UTM

- Nano UTM has a large dynamic range

  Max load---500 mN with 50 nN res.

  Max elong.---150 mm with 35 nm res.

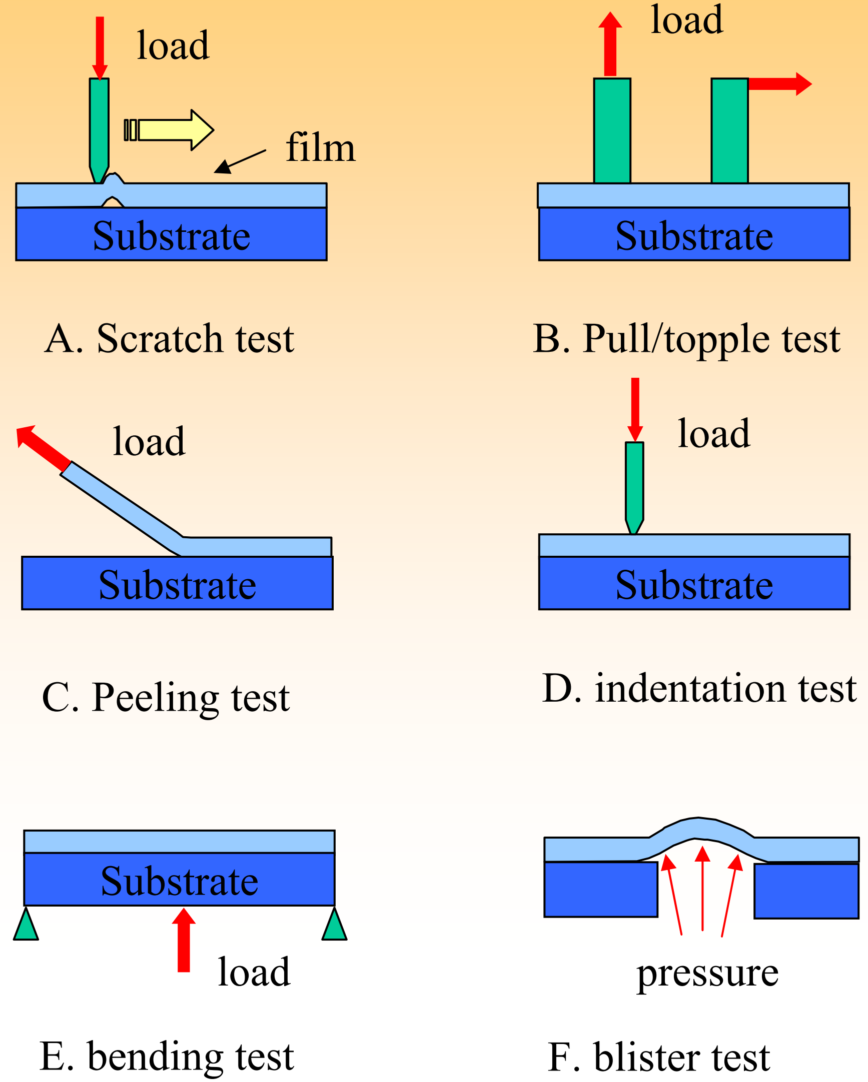
  Dynamic freq. range--- 0.1 to 2500Hz

Application: Tensile, Compression, fatigue, Four-Point Bend, Dynamic Mechanical Analysis, Special geometries - component testing (e.g., MEMS)

Current evaluation methods of interfacial strength

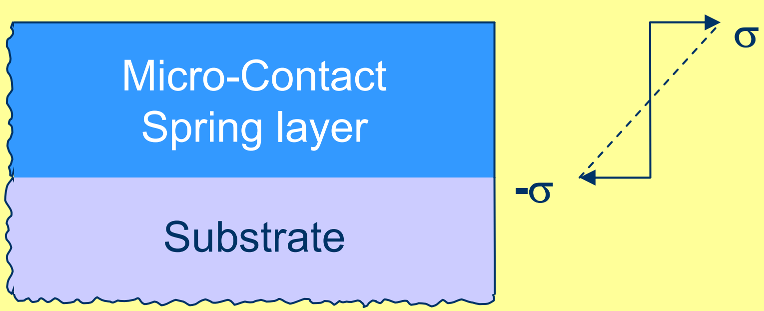
Limitations of current methods

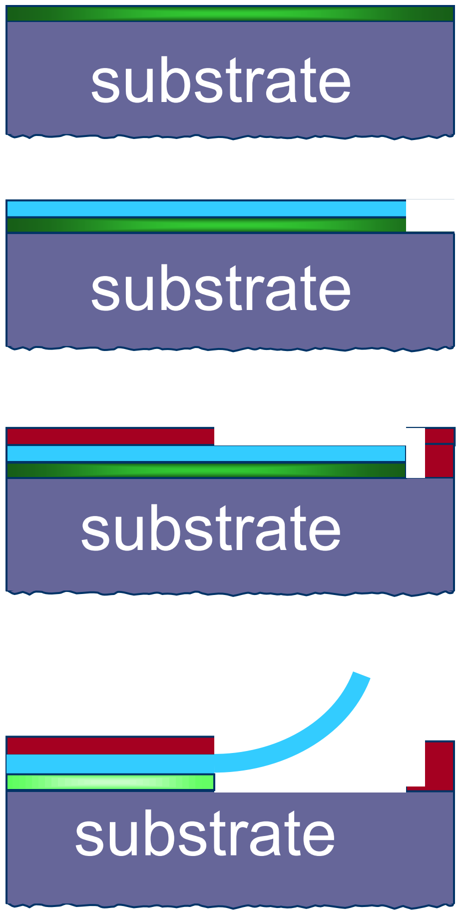
- Can not provide the mode mix, fabrication process dependent toughness inexpensively and efficiently
- Large plasticity associated with these methods makes the results difficult to deconvolute.
- Bad repeatability for some tests.
- In process monitoring impossible.
- Limited mode mixity
- Hard to handle the sample in some test



Micro-contact Spring Fabrication

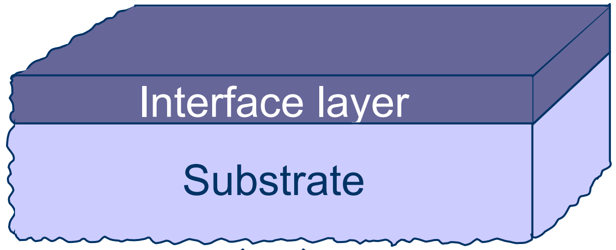
- Thin film metal intrinsic stress can be controlled by varying the DC sputter chamber pressure
  - Low pressure: “Shot-peening” mechanism causes compressive stresses
  - High pressure: Interatomic attractions in porous microstructure causes tensile stress

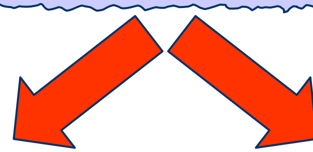




Method Concept

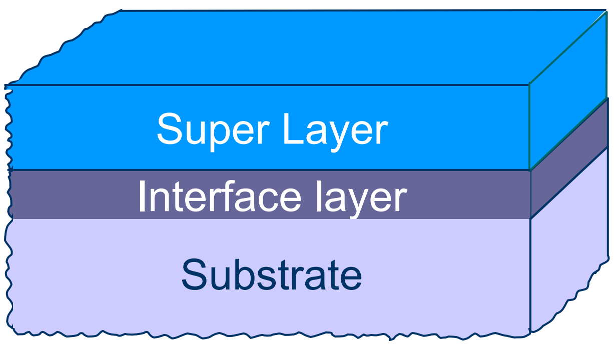
$$G = -\frac{dU}{dA}$$





Change dU

(Vary h_{sp} or σ_{sp})

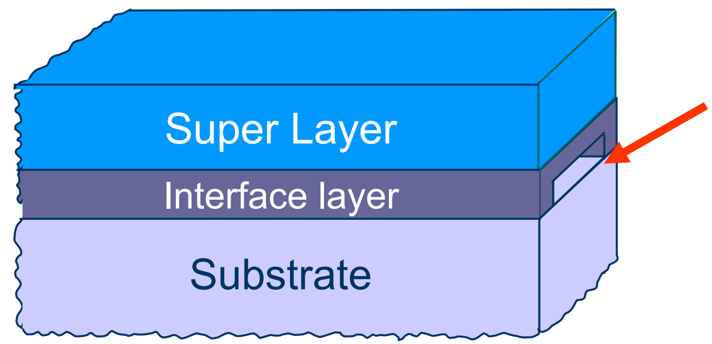


Decohesion test of Bagchi (1994)

Requires multiple samples, each with different dU

Change dA

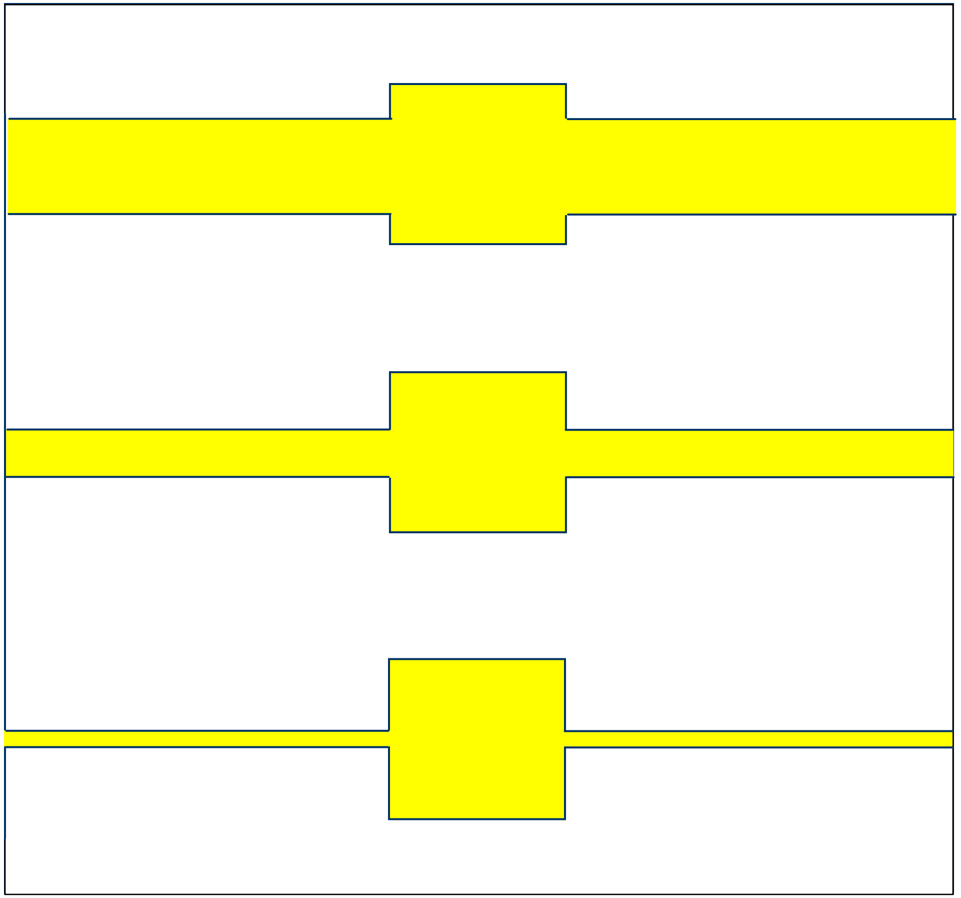
(Vary area interface layer touches substrate)



Modified Decohesion Test (MDT)

Requires only 1 Sample!!!!

MDT Implementation: Step 1

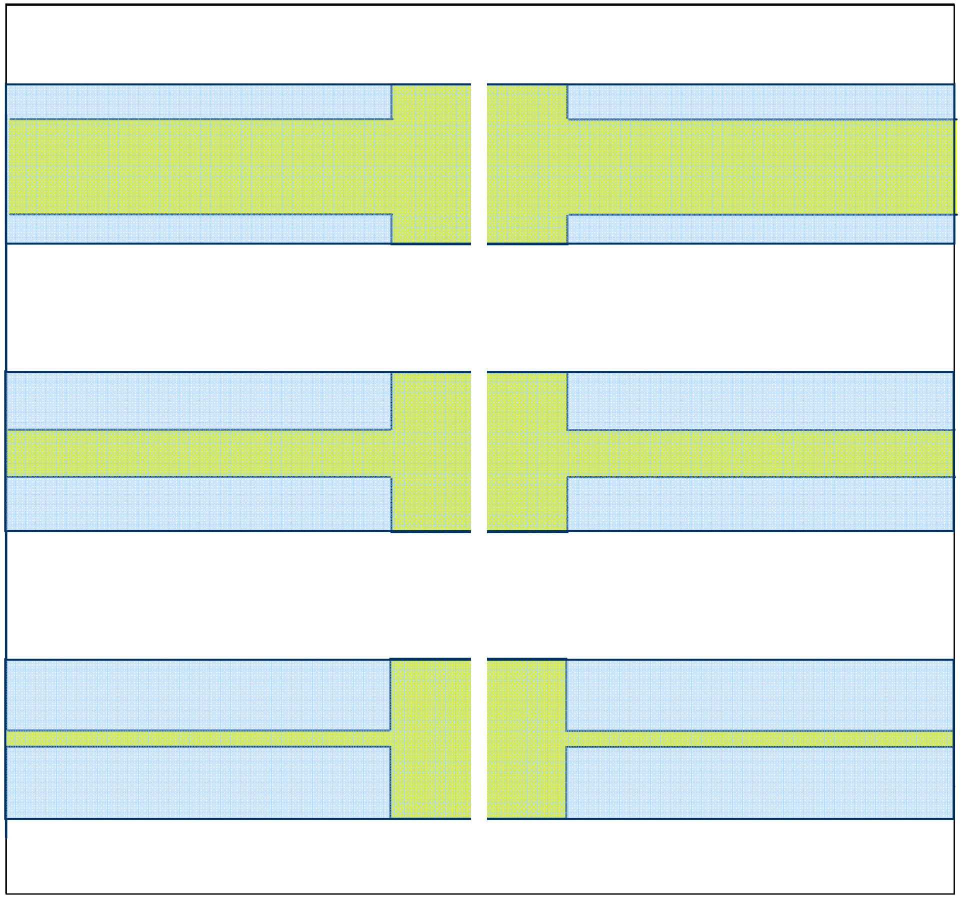


- Start with a bare substrate
- Deposit a “Non-Adhesive” layer
- Pattern into horizontal strips with varying widths

MDT Implementation: Step 2

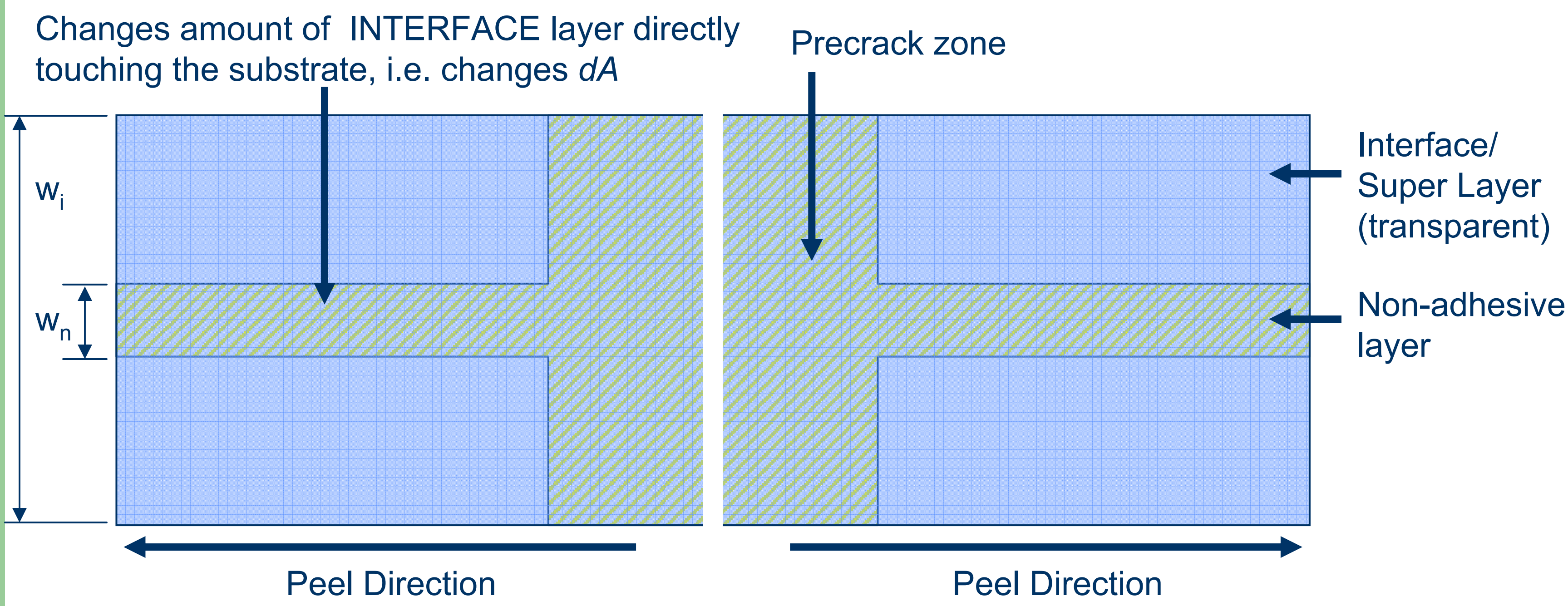
- Start with a bare substrate
- Deposit a “Non-Adhesive” layer
- Pattern into horizontal strips with varying widths
- Deposit an “Interface” layer
- Deposit an intrinsically stressed “Super” layer
- Pattern into strips that blanket the Non-adhesive layer strips

MDT Implementation: Step 3



- Start with a bare substrate
- Deposit a “Non-Adhesive” layer
- Pattern into horizontal strips with varying widths
- Deposit an “Interface” layer
- Deposit an intrinsically stressed “Super” layer
- Pattern into strips that blanket the Non-adhesive layer strips
- Cut the strips to initiate a crack

MDT Implementation: Close Up

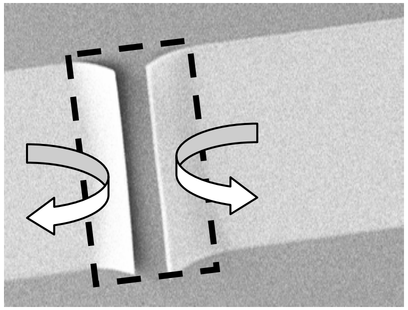


G scales with ζ

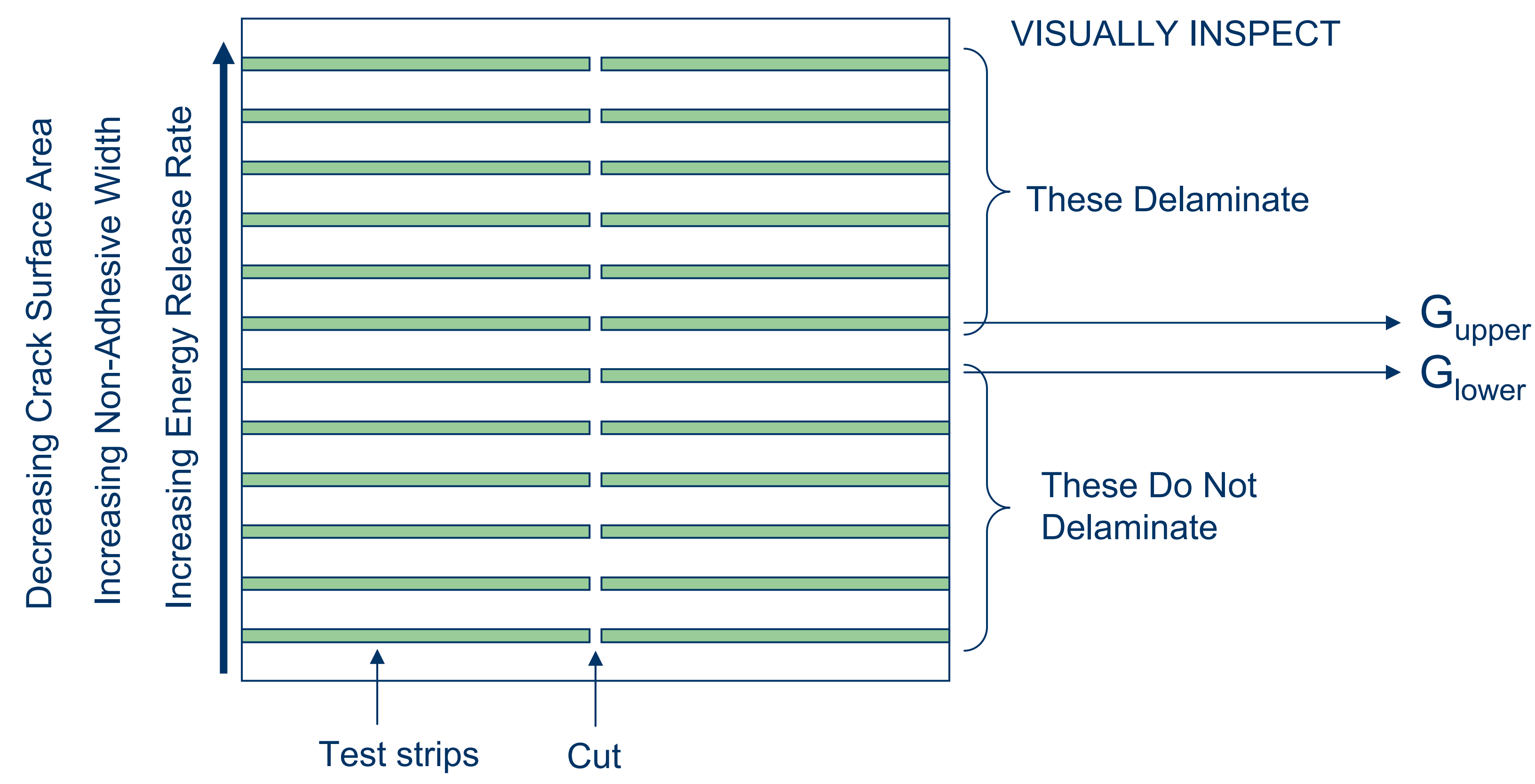
$$\zeta = \frac{w_n}{w_i} \longrightarrow G = G_o M = G_o (1-\zeta)^{-1}$$

G_o calculated by VKPT-MT

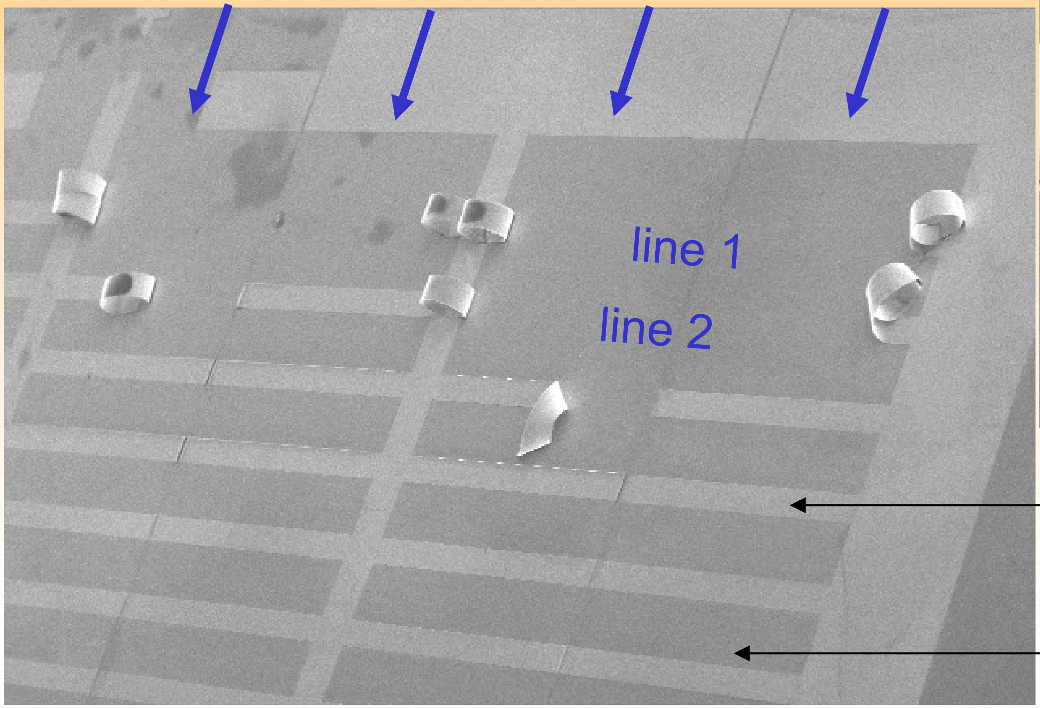
SEM of precrack

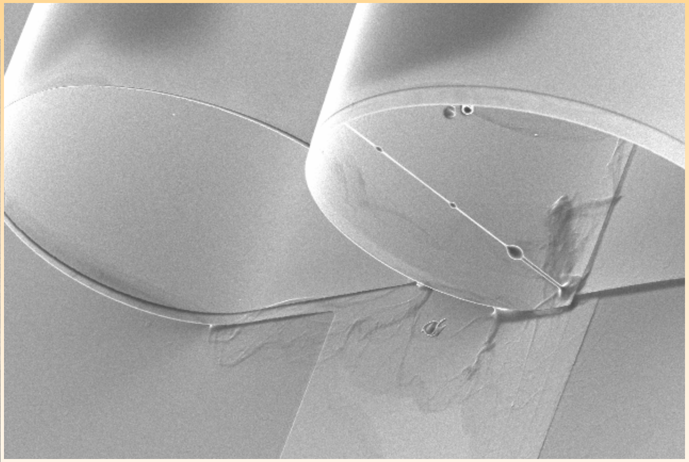


MDT Implementation: Conclusion



Delaminated Interfaces

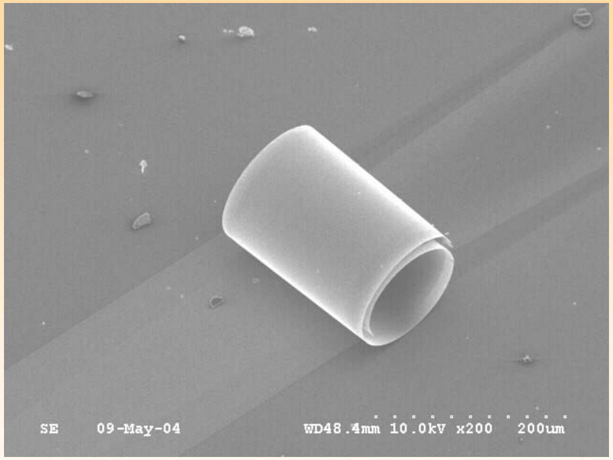


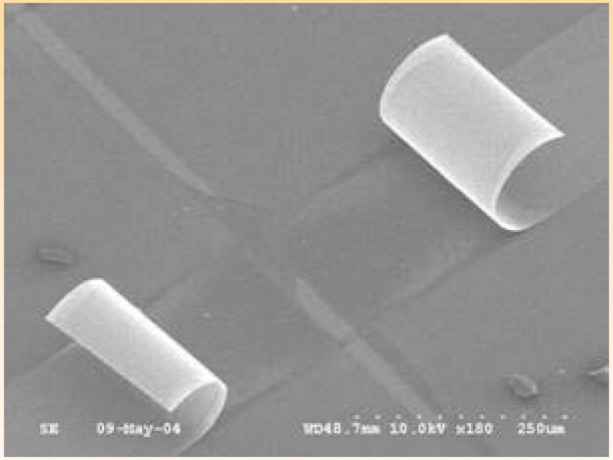


SEM Picture of test sample #43

Modi, M and Sitaraman, S. K., "Interfacial fracture toughness measurement for thin film interfaces," Engineering Fracture Mechanics, Vol. 71, 2004, pp. 1219-1234.

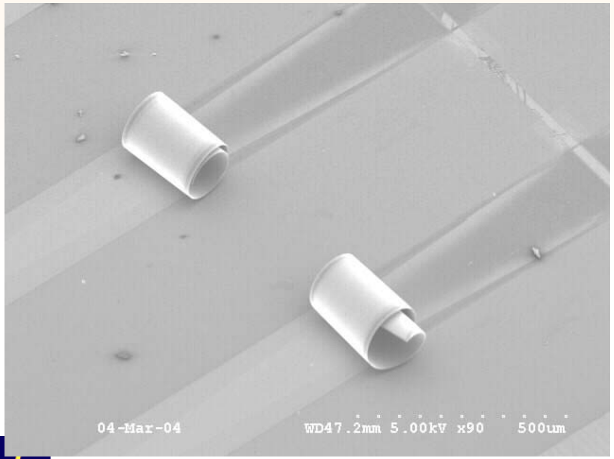
SEM images of Delaminated Ti/Si Interface

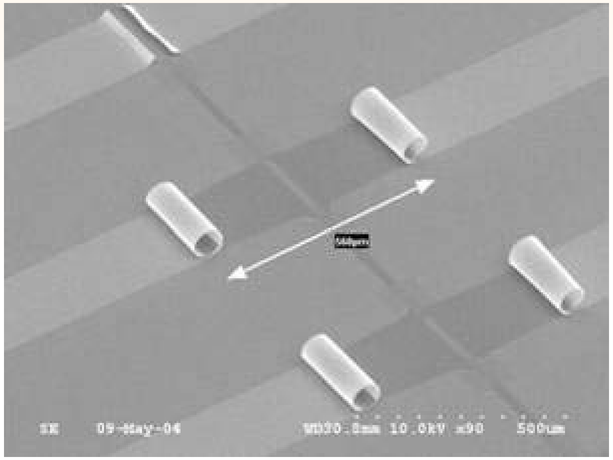




DC sputtered Ti on silicon substrate
Ti thickness: ~100nm

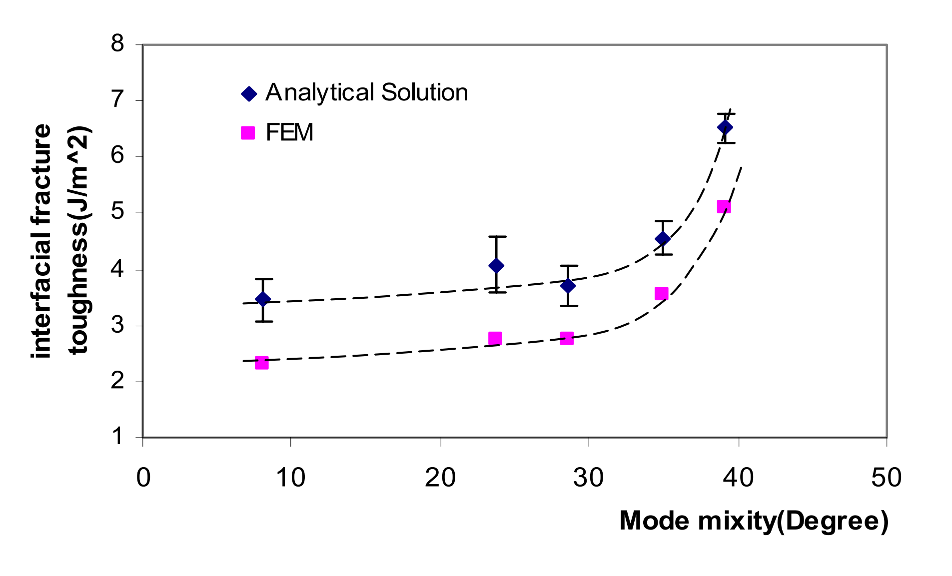
DC sputtered Cr:
Cr Thickness: ~50nm–500nm
Cr intrinsic stress: 1.017 GPa

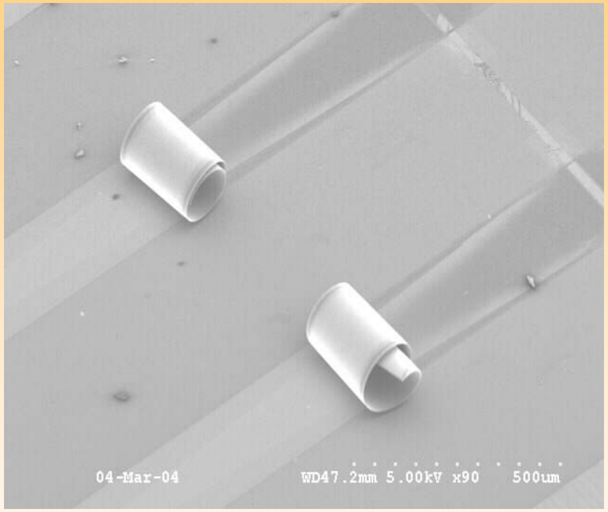




The particles are from the dicing of the sample by diamond scriber

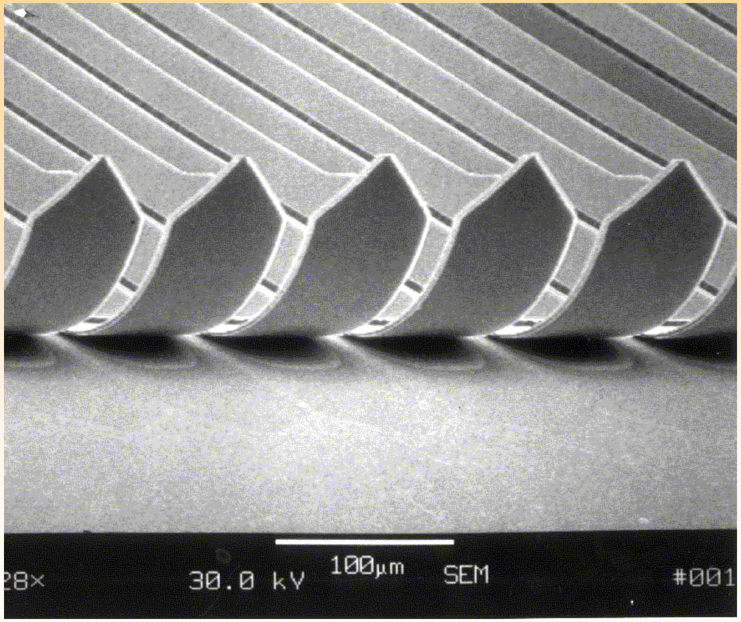
Fracture Toughness Results

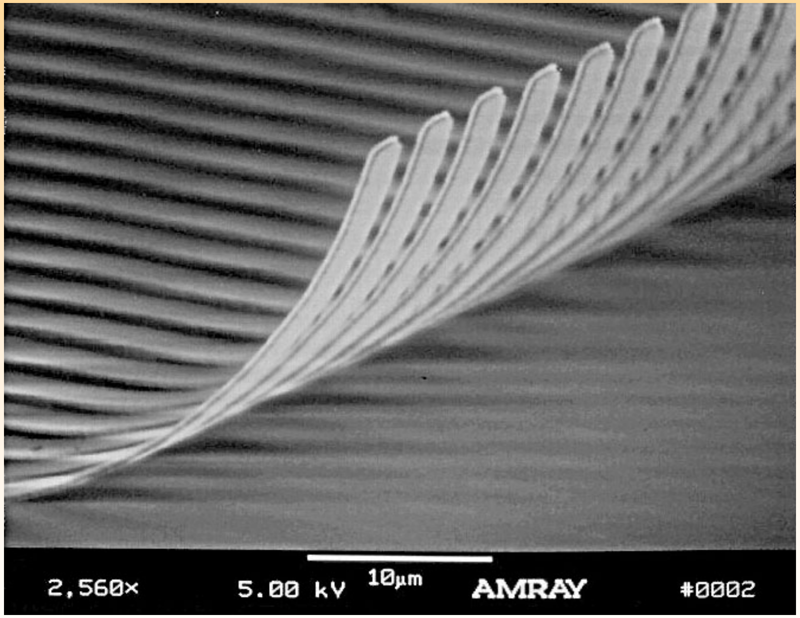




Ti thickness (nm)	Cr thickness (nm)	Mode mixity (°)	Γ (analytical method) (J/m²)	Γ (FEM) (J/m²)
87	50	8.07	3.45	2.33
87	150	23.7	4.08	2.75
87	200	28.5	3.72	2.74
87	300	35.0	4.55	3.55
87	400	39.1	6.51	5.09

Micro-contact springs at 80 µm pitch and 6 µm pitch






IEEE TRANSACTIONS ON
ADVANCED PACKAGING
A PUBLICATION OF THE IEEE COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY SOCIETY
AND THE LASERS AND ELECTRO OPTICS SOCIETY
WWW.CPMT.ORG
CPMT
IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY
MAY 2003
VOLUME 26
NUMBER 2
ITAPFZ
(ISSN 1521-3323)
IEEE

Ongoing Work

- Alternate interconnect materials
- Alternate interconnect geometries
- Finer-pitch interconnects fabrication
- More electrical studies
- More assembly and reliability testing
- Thin-film materials characterization- more advanced techniques

Computer-Aided Simulation of Packaging Assembly and Reliability (CASPAR)-MARC 360

- Dr. Suresh Sitaraman
- Mr. Jamie Ahmad, MSME Student
- Mr. Mudasir Ahmad, MSME
- Mr. Francis Classe, MSME
- Ms. Jill Conley, MSME
- Mr. Rafael de Cardenas, MSME
- Mr. Manoj Damani, MSME Student
- Mr. Rajiv Dunne, PhD
- Mr. Joe Haemer, MSME
- Mr. Carlton Hanna, MSME
- Mr. Rich Harries, MSME
- Mr. Shashi Hegde, PhD Student
- Dr. Hurang Hu, Post-Doc
- Mr. Karan Kacker, MSME Student
- Dr. Yeong Kim, Post-Doc
- Mr. Kevin Klein, MSME Student
- Mr. K. J. Lee, MSME Student
- Mr. George Lo, MSME Student
- Mr. Lunyu Dennis Ma, PhD
- Mr. Saketh Mahalingam, PhD Student
- Mr. Hernan Mercado, MSME
- Mr. Stelios Michaelides, PhD
- Mr. Mitul Modi, PhD
- Mr. Sean Murphy, MSME
- Mr. Andy Perkins, PhD Student
- Dr. Raghuram Pucha, Post-Doc
- Mr. James Pyland, MSME Student
- Mr. Rajiv Raghunathan, MSME
- Mr. Gyan Ramakrishna, MSME
- Dr. Zhaohui Shan, Post-Doc
- Mr. Jorg Sizemore, MSME
- Mr. Kyle Smith, MSME
- Ms. Uramella Suljuzovic, MSME
- Dr. Vish Sundararaman, Post-Doc
- Ms. Manjula Surendran, MSME
- Mr. Krishna Tunga, MSME Student
- Mr. Weidong Xie, PhD
- Mr. Jiantao Zheng, PhD Student
- Ms. Angela Qi Zhu, PhD
- Several Undergraduate Students